What is claimed is:

1. A checkerboard buffer page system, comprising:

a data source, providing data elements in a first order;

a data destination, receiving data elements in a second order;

at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored in parallel to the memory devices and retrieved in parallel from the memory devices; and

where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and at least one entry in each buffer page corresponds to a data element,

where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order,

where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and

where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

2. The checkerboard buffer page system of claim 1, where each memory page corresponds to a respective buffer page.

3. The checkerboard buffer page system of claim 1, where a data element is pixel data corresponding to a pixel in a frame of pixels, the frame having horizontal rows of pixels and vertical columns of pixels.

4. The checkerboard buffer page system of claim 3, where each row of the frame includes 1920 pixels and each column of the frame includes 1080 pixels.

5. The checkerboard buffer page system of claim 3, where each pixel has 32 bits of pixel data.

6. The checkerboard buffer page system of claim 3, where the buffer pages are pixel pages, each pixel page having a plurality of pixel page rows and a plurality of pixel page columns.

7. The checkerboard buffer page system of claim 6, where:

a first number of pixel pages are allocated horizontally to include all of the pixels in a horizontal row of pixels in the frame,

a second number of pixel pages are allocated vertically to include all of the pixels in a vertical column of pixels in the frame, and

a total number of pixel pages are allocated to include all of the pixels in the frame, and the total number is equal to the product of the first number and the second number.

8. The checkerboard buffer page system of claim 7, where the first number is 120.

9. The checkerboard buffer page system of claim 7, where the first number is 60.

10. The checkerboard buffer page system of claim 7, where the second number is 68.

11. The checkerboard buffer page system of claim 6, where addresses for storing and retrieving pixel data are generated using one or more counter variables.

12. The checkerboard buffer page system of claim 11, where counter variables include:

a pixel page column variable for counting pixel page columns;

a pixel page row variable for counting pixel page rows;

a pixel page horizontal variable for counting pixel pages horizontally; and

a pixel page vertical variable for counting pixel pages vertically.

13. The checkerboard buffer page system of claim 11, where at least one counter variable is a counter.

14. The checkerboard buffer page system of claim 11, where addresses for storing pixel data are generated according to horizontal rows of pixels.

15. The checkerboard buffer page system of claim 11, where addresses for retrieving pixel data are generated according to vertical columns of pixels.

16. The checkerboard buffer page system of claim 6, further comprising a memory controller for generating addresses for storing and retrieving data elements.

17. The checkerboard buffer page system of claim 16, where:

the at least two memory devices comprises a first memory device and a second memory device,

the memory controller has two states for storing data for a horizontal pixel pair, where a first pixel in the horizontal pixel pair is horizontally adjacent and to the left of a second pixel in the horizontal pixel pair: a first state where pixel data for the first pixel in the horizontal pixel pair is stored to the first memory device and pixel data for the second pixel in the horizontal pixel pair is stored to the second memory device; and a second state where pixel data for the first pixel in the horizontal pixel pair is stored to the second memory device and pixel data for the second pixel in the horizontal pixel pair is stored to the first memory device, and

the memory controller changes states for storing data after storing pixel data for one horizontal row of pixels.

18. The checkerboard buffer page system of claim 16, where:

the at least two memory devices comprises a first memory device and a second memory device,

the memory controller has two states for retrieving data for a vertical pixel pair, where a first pixel in the vertical pixel pair is vertically adjacent and above a second pixel in the vertical pixel pair: a first state where pixel data for the first pixel in the vertical pixel pair is retrieved from the first memory device and pixel data for the second pixel in the vertical pixel pair is retrieved from the second memory device; and a second state where pixel data for the first pixel in the vertical pixel pair is retrieved from the second memory device and pixel data for the second pixel in the vertical pixel pair is retrieved from the first memory device, and

the memory controller changes states for retrieving data after retrieving pixel data for one vertical column of pixels.

19. The checkerboard buffer page system of claim 18, where:

pixel data for the first pixel in the vertical pixel pair is retrieved using a first address,

pixel data for the second pixel in the vertical pixel pair is retrieved using a second address,

in the first state for retrieving data, the first address is provided to the first memory device and the second address is provided to the second memory device, and

in the second state for retrieving data, the first address is provided to the second memory device and the second address is provided to the first memory device.

20. A checkerboard pixel page system, comprising:

a video source providing pixel data for pixels in a frame, the frame having rows of pixels and columns of pixels;

a video destination;

a first memory having a plurality of memory locations;

a second memory having a plurality of memory locations;

a memory controller connected to the first memory and the second memory;

a first data bus connected to the video source and the memory controller;

a second data bus connected to the video source and the memory controller;

a third data bus connected to the video destination and the memory controller;

a fourth data bus connected to the video destination and the memory controller;

a source address line connected to the video source and the memory controller; and

a destination address line connected to the video destination and the memory controller,

where each pixel corresponds to an entry in one of a plurality of pixel pages, and a pixel page includes multiple pixels from a row in the frame and multiple pixels from a column in the frame, and each pixel page includes at least one pixel in the frame,

where each entry in a pixel page corresponds to a memory location,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memories, and

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memories.

21. The checkerboard pixel page system of claim 20, where the memory controller generates addresses for storing and retrieving pixel data.

22. The checkerboard pixel page system of claim 21, where:

the memory controller has two states for storing data for a horizontal pixel pair, where a first pixel in the horizontal pixel pair is horizontally adjacent and to the left of a second pixel in the horizontal pixel pair: a first state where pixel data for the first pixel in the horizontal pixel pair is stored to the first memory and pixel data for the second pixel in the horizontal pixel pair is stored to the second memory; and a second state where pixel data for the first pixel in the horizontal pixel pair is stored to the second memory and pixel data for the second pixel in the horizontal pixel pair is stored to the first memory, and

the memory controller changes states for storing data after storing pixel data for one horizontal row of pixels.

23. The checkerboard pixel page system of claim 21, where:

the memory controller has two states for retrieving data for a vertical pixel pair, where a first pixel in the vertical pixel pair is vertically adjacent and above a second pixel in the vertical pixel pair: a first state where pixel data for the first pixel in the vertical pixel pair is retrieved from the first memory and pixel data for the second pixel in the vertical pixel pair is retrieved from the second memory; and a second state where pixel data for the first pixel in the vertical pixel pair is retrieved from the second memory and pixel data for the second pixel in the vertical pixel pair is retrieved from the first memory, and

the memory controller changes states for retrieving data after retrieving pixel data for one vertical column of pixels.

24. The checkerboard pixel page system of claim 23, where:

pixel data for the first pixel in the vertical pixel pair is retrieved using a first address,

pixel data for the second pixel in the vertical pixel pair is retrieved using a second address,

in the first state for retrieving data, the first address is provided to the first memory and the second address is provided to the second memory, and

in the second state for retrieving data, the first address is provided to the second memory and the second address is provided to the first memory.

25. The checkerboard pixel page system of claim 20, where addresses for storing and retrieving pixel data are generated using one or more counter variables.

26. The checkerboard pixel page system of claim 25, where counter variables include:

a pixel page column variable for counting pixel page columns;

a pixel page row variable for counting pixel page rows;

a pixel page horizontal variable for counting pixel pages horizontally; and

a pixel page vertical variable for counting pixel pages vertically.

27. The checkerboard pixel page system of claim 25, where at least one counter variable is a counter.

28. The checkerboard pixel page system of claim 25, where addresses for storing pixel data are generated according to horizontal rows of pixels.

29. The checkerboard pixel page system of claim 25, where addresses for retrieving pixel data are generated according to vertical columns of pixels.

30. A method of storing pixel data, comprising:

receiving pixel data for a frame of pixels, where the frame includes multiple horizontal rows of pixels; and

storing the pixel data in a memory system according to pixel pages,

where each pixel page corresponds to a respective page of memory, at least one pixel page includes pixels from multiple horizontal rows of pixels, and each pixel page includes at least one pixel,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memory system, and

where pixel data for neighboring pixels horizontally and vertically adjacent to a reference pixel, within the same pixel page as the reference pixel, is stored in a different memory than pixel data for the reference pixel.

31. The method of claim 30, further comprising:

providing pixel data for two pixels from a video source to a memory controller;

generating a source address in the memory controller, where the source address is a memory address for storing the pixel data for two pixels;

providing the pixel data for two pixels to the memory system;

providing the source address to the memory system; and

storing the pixel data for two pixels in the memory system at the source address.

32. The method of claim 30, where addresses for storing pixel data are generated using one or more counter variables.

33. The method of claim 32, where counter variables include:

a pixel page column variable for counting pixel page columns;

a pixel page row variable for counting pixel page rows;

a pixel page horizontal variable for counting pixel pages horizontally; and

a pixel page vertical variable for counting pixel pages vertically.

34. The method of claim 33, where generating addresses comprises:

outputting an address;

incrementing the address;

incrementing the pixel page column variable;

comparing the pixel page column variable to half of the width of one pixel page;

comparing the pixel page column variable to the width of one pixel page;

comparing the pixel page horizontal variable to the number of pixel pages allocated horizontally for one frame;

comparing the pixel page row variable to the height of one pixel page; and

comparing the pixel page vertical variable to the number of pixel page allocated vertically for one frame.

35. A method of retrieving pixel data, comprising:

generating addresses for retrieving from a memory system pixel data for a frame of pixels according to pixel pages, where the frame includes multiple horizontal rows of pixels, where each pixel page corresponds to a respective page of memory, where at least one pixel page includes pixels from multiple horizontal rows of pixels, and where each pixel page includes at least one pixel; and

retrieving the pixel data from the memory system using the generated addresses, where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memory system, and

where pixel data for neighboring pixels horizontally and vertically adjacent to a reference pixel, within the same pixel page as the reference pixel, is retrieved from a different memory than pixel data for the reference pixel.

36. The method of claim 35, further comprising:

generating two destination address in a memory controller, where the destination addresses are memory addresses for retrieving pixel data;

providing the two destination addresses to the memory system; and

providing pixel data from the memory system stored at the two destination addresses to the memory controller.

37. The method of claim 35, where addresses for retrieving pixel data are generated using one or more counter variables.

38. The method of claim 37, where counter variables include:

a pixel page column variable for counting pixel page columns;

a pixel page row variable for counting pixel page rows;

a pixel page horizontal variable for counting pixel pages horizontally; and

a pixel page vertical variable for counting pixel pages vertically.

39. The method of claim 38, where generating addresses comprises:

outputting an address;

incrementing the address;

incrementing the pixel page row variable;

comparing the pixel page row variable to half of the height of one pixel page;

comparing the pixel page row variable to the height of one pixel page;

comparing the pixel page vertical variable to the number of pixel pages allocated vertically for one frame;

comparing the pixel page column variable to the width of one pixel page; and

comparing the pixel page horizontal variable to the number of pixel page allocated horizontally for one frame.

40. A system for storing pixel data, comprising:

means for receiving pixel data for a frame of pixels, where the frame includes multiple horizontal rows of pixels; and

means for storing the pixel data in a memory system according to pixel pages,

where each pixel page corresponds to a respective page of memory, at least one pixel page includes pixels from multiple horizontal rows of pixels, and each pixel page includes at least one pixel,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memory system, and

where pixel data for neighboring pixels horizontally and vertically adjacent to a reference pixel, within the same pixel page as the reference pixel, is stored in a different memory than pixel data for the reference pixel.

41. A system for retrieving pixel data, comprising:

means for generating addresses for retrieving from a memory system pixel data for a frame of pixels according to pixel pages, where the frame includes multiple horizontal rows of pixels, where each pixel page corresponds to a respective page of memory, where at least one pixel page includes pixels from multiple horizontal rows of pixels, and where each pixel page includes at least one pixel; and

means for retrieving the pixel data from the memory system using the generated addresses,

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memory system, and

where pixel data for neighboring pixels horizontally and vertically adjacent to a reference pixel, within the same pixel page as the reference pixel, is retrieved from a different memory than pixel data for the reference pixel.